ECE Fundamentals III Final Project

Super myRios Bros

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Brandon Chan (bc5fg) : Component Calculation and Simulations
Mesgana Dinare (md5jd) : Soldering and Test Subject
Ashley Ferraro (cbf6yd) : Component Calculation and Design Verification
Kwadwo Tenkorang (knt4xx) : Initial Design and Circuit Debugging

“On my honor, as a student, I have neither given nor received aid on this assignment/exam”

Calculations and Design

Background

Motivation and Approach

The goal of this project is to build a working electrocardiogram (EKG). An EKG is a piece of medical equipment that measures the electrical activity of the heart and can be used to diagnose various heart conditions.The EKG has three inputs connected to the body, two to the arms for measuring the actual signals and and one to the ankle that grounds the system. The EKG signal is then converted into an electrical signal that can be captured with a VirtualBench or digitally filtered through a microcontroller like a myRIO or an MSP430.

Since the input signals to the EKG are in the order of micro volts, they will first need to be filtered to remove as much noise as possible and passed through an instrumentation amplifier to amplify them to levels where they can be read by the VirtualBench and other devices. In order to prepare the system for digital signal processing (DSP), an antialiasing filter will be designed to attenuate all frequencies higher than desired in order to meet the Nyquist Theorem. Additionally, since the system will be interacting with various devices such as the myRIO or MSP430, which have different grounds, galvanic isolation will be used to prevent unwanted current flow between the two systems.

The entire system will have several options for power input: 9V battery, myRIO and MSP430. All of these signals will be brought to 3.3V, which will be used to power the various operational amplifiers, instrumental amplifiers and optoisolators.

Expected Input and Required Gain

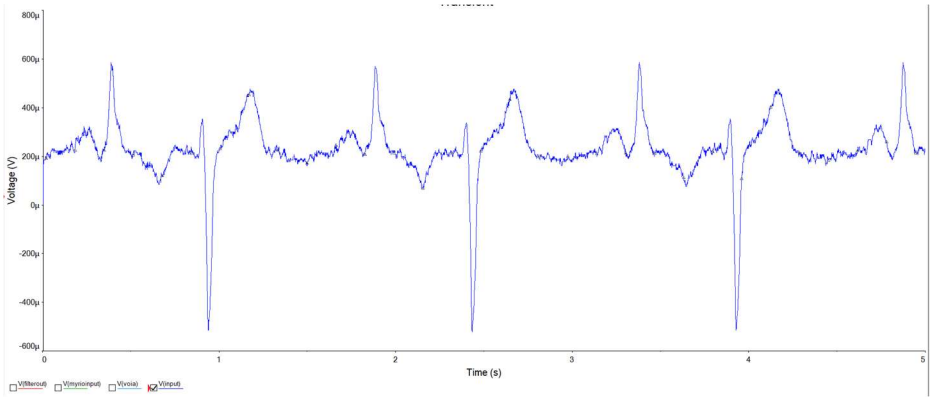

Figure 1.0: Simulated Heartbeat

This simulated heartbeat that was given shows the correct voltages ranges, -600 to 600uV with a DC offset of about 200uV. However, these voltages are too low for the virtual bench to accurately read so the instrumentation amplifier was added. This causes the signal to have a

gain of about 1000 and output a heartbeat signal with a voltage that ranges from -600mV to 600mV roughly.

Filter Requirements

A lowpass filter was implemented to eliminate signals above 500Hz, this is to make sure that there was no aliasing with the myRio. This is because the myRio has a sampling frequency of 1kHz and to make sure there is no aliasing, there should be no signal above 500Hz.

Schematic

Subsystem: Input

The input subsystem is composed of an RC network, instrumental amplifier and integrator.

RC Network

To begin the design process, the RC Network was created first:

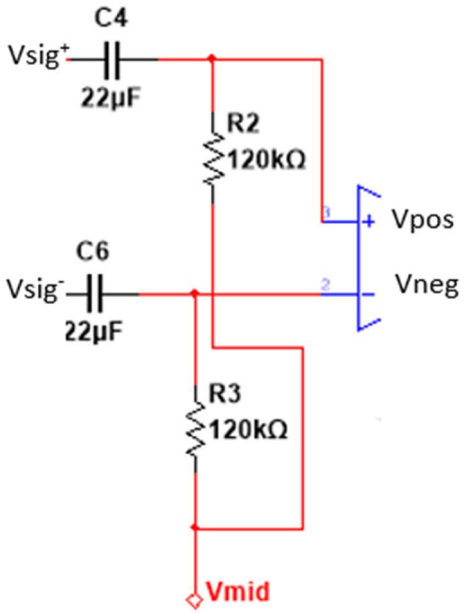

Figure 1.1: RC Network

Given that the RC network which feeds into the IAMP are high pass filters, they have the following transfer functions:

$$\frac{V_{pos}}{V_{sig}+} = \frac{s}{s+\frac{1}{R2C4}} \qquad \frac{V_{neg}}{V_{sig}-} = \frac{s}{s+\frac{1}{R3C6}}$$

Given the following constraint on the corner frequencies for both sections, $0.05 \leq f_c \leq 0.1\ Hz$and that the corner frequency for each section is:

$$2\pi f_c = w_c = \frac{1}{R_2 C_4} = \frac{1}{R_3 C_6}$$

Using a MATLAB script, we solved for R2=R3=120kΩ and C4=C6=22μF.

Instrumentation Amplifier Gain Resistor

The input signal originally has a pk-pk amplitude of 600 μV; to get a valid output, the following equations is used,

$$\frac{Vout}{Vin} = 1 + \frac{100k}{R_G}$$

where R_G is the gain resistor. Since Vout/Vin = 2V/600μV, we need a gain of about 3000. However according to the Iamp datasheet, Iamp's have a maximum gain of 1000, so the value of R_G has to be 100Ω.

Integrator

After designing the RC network, we moved onto designing the integrator to track the output of the Iamp.

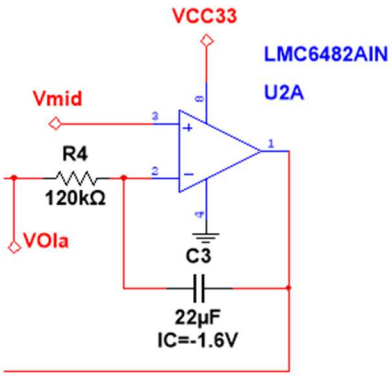

Figure 1.2: Integrator

The design constraints as outlined from the project is that the values of the integrator must be picked such that the transfer function of the integrator is shown to be:

$$\frac{-1}{s} \leq H(s) \leq \frac{-1}{10s}$$

Due to the transfer function of an integrator being the following: $H(s) = \frac{-1}{RCs}$the product of *R* and *C* must be between 1 and 10. Utilizing a MATLAB script, we found R4 to be 120 kΩ and C3 to be 22 μF as the product of these values fit within the aforementioned range:

$$H(s) = \frac{-1}{120000 \cdot 22 \cdot 10^{-6} s} = \frac{-1}{2.6364s}$$

This thus concludes the design process for the integrator.

Subsystem: Power (VMID)

For the design of VMID to half the 3.3V input we began by simplifying the circuit shown in Figure 1.3.

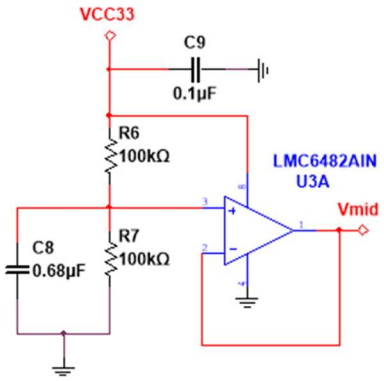

Figure 1.3: VMID Topology

Using a Thevenin equivalent resistance given that capacitors at DC are open circuits and power sources are ground, R6 is in parallel with R7 and thus the resistance is shown to be:

$$R_{eq} = \frac{R6R7}{R6+R7}$$

Given that the topology is high pass and the constraints of the circuit are what is shown below:

$$25k\Omega < R_{eq} < 100k\Omega$$
$$2\ Hz < f_c < 5\ Hz$$
$$f_c = \frac{1}{2\pi R_{eq} C}$$

Using a MATLAB script to iterate through available capacitors and resistors with these constraints, it was determined R6=R7=100kΩ and C8=0.68µF.

Subsystem: Anti-Aliasing Filter

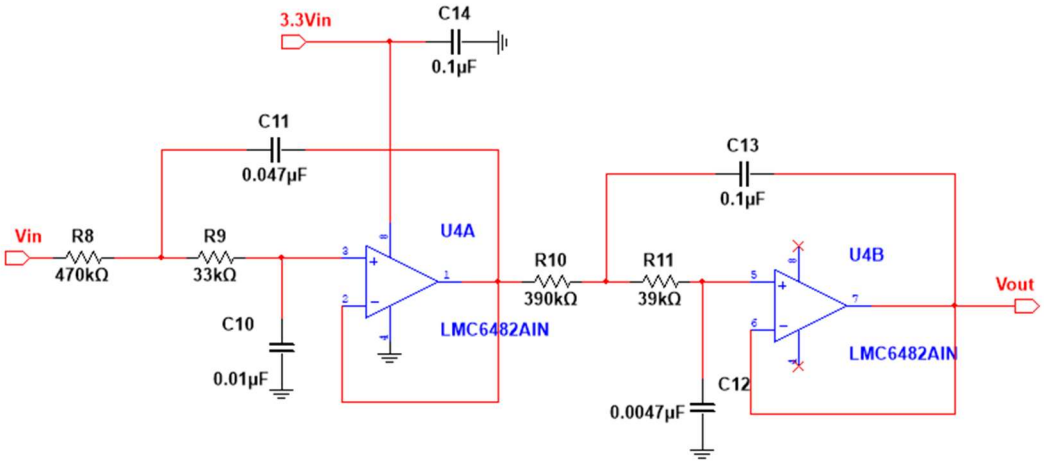

Figure 1.4: Antialias Filter

Given the initial constraints of -72dB at 500Hz, and designing a 4th order Buttersworth, we used the following relationship to determine the cutoff frequency for each filter.

$$\frac{f_{max}}{fc} = 10^{\frac{G_{stop}-G}{20N}}$$

Where $f_{max} = 500Hz, G_{stop} = 60dB, G = 0, (for\ unity\ gain)\ and\ N = 4$, and solving for $f_c = 63Hz$. Thus we designed two butterworth lowpass filters in unity gain configurations with two different Q factors of Q_1=0.5412 and Q_2=1.3065 since their product is 0.707. Resistor and capacitor values were determined using the ratio method. Simplification 3.2 from the TI document was used:

$$R1 = mR, R2 = R, C1 = C, C2 = nC\ and\ K = 1\ resulting\ in\ f_c = \frac{1}{2\pi RC\sqrt{mn}}\ and\ Q = \frac{\sqrt{mn}}{m+1}$$

The lowest Q was assigned to the first filter in the sequence.

First Stage: Q_1=0.5412
Fixing R9 at a value from out kit, R9=33kΩ and using an m=14, we determined n=4.7 and that R8=470kΩ. Given this information and a corner frequency of 63Hz, C10 was solved for. The closest capacitor value available to us for C10=0.01µF and using n=4.7, the closest capacitor value for C11=0.047µF.

Second Stage: Q_2=1.3065

Looking at resistor and capacitor values we had available to us we fixed R11=39kΩ and using an m=10, we determined n=20 and that R10=390kΩ. Given this information and a corner frequency of 63Hz C12=C can be solved for. The closest value in our kit is C12 = 0.0047μF, and using the value of n, the closest kit capacitor for C13 = 0.1μF.

Subsystem: Isolator

To begin designing the Isolator, we consulted the datasheet for the component properties. We noted that the servo gain, the ratio between the current for the photocurrent, I_{P1} and the current to drive the LED, I_F is $K1 = \frac{I_{P1}}{I_f}$and that this value was constrained by $0.006 < \frac{I_{P1}}{I_f} < 0.017$ given I_F=10mA.

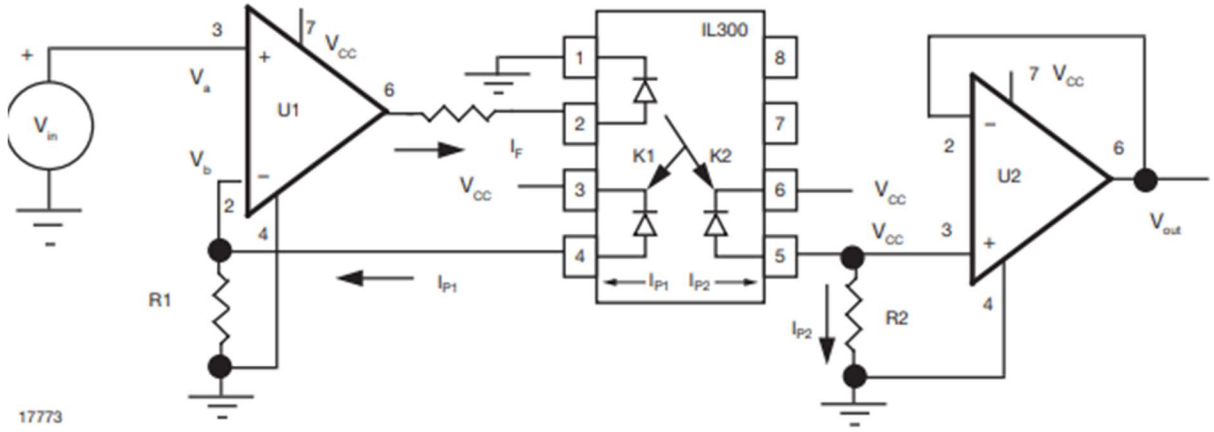

Figure 1.5: Isolator Configuration (From Datasheet)

Ratio K2 is determined similarly and the ratio is shown to be R3 = R1/R2. The design for the isolator has gain $G = K3\frac{R2}{R1}$. Given this information that the isolator must have unity gain, the following assumption can be made that R12=R13.

The design constraint that the max current designed to the input amp of the LED is less than 10mA. Additionally, the max voltage input for the LED is 3.3V and the voltage needed to turn the LED on is 1.5V. Given this information and using the value of resistor R13 the LED max current can be found using Ohm's law:

$$I_{max} > \frac{V_{in} - V_{LED}}{R13}$$

Thus R13 > 180Ω, thus we chose R13=220Ω. Simplifying the original constraint of K1 given that the max LED current I_F=10mA, $0.00006A < I_{P1} < 0.00017A$.Given that the output voltage $V_{out} = I_{P1}R14$ and that V_{out} should be unity with the input which has a max of 3.3V, $I_{P1}R14 < 3.3V$. Using the worst case LED current 0.00006A, 0.00006R14 < 3.3V, R14=R12 < 55kΩ. Thus we chose R12=R14=47kΩ.

Multisim Simulations

Time Domain

The image below displays the EKG input signal and since the y-axis is very small (microvolts), a voltage gain needs to be applied onto the signal in order for the original signal to be viewable on the VirtualBench. This is to simulate when retrieving the heartbeat signal from a person as this signal is also on the microvolts scale.

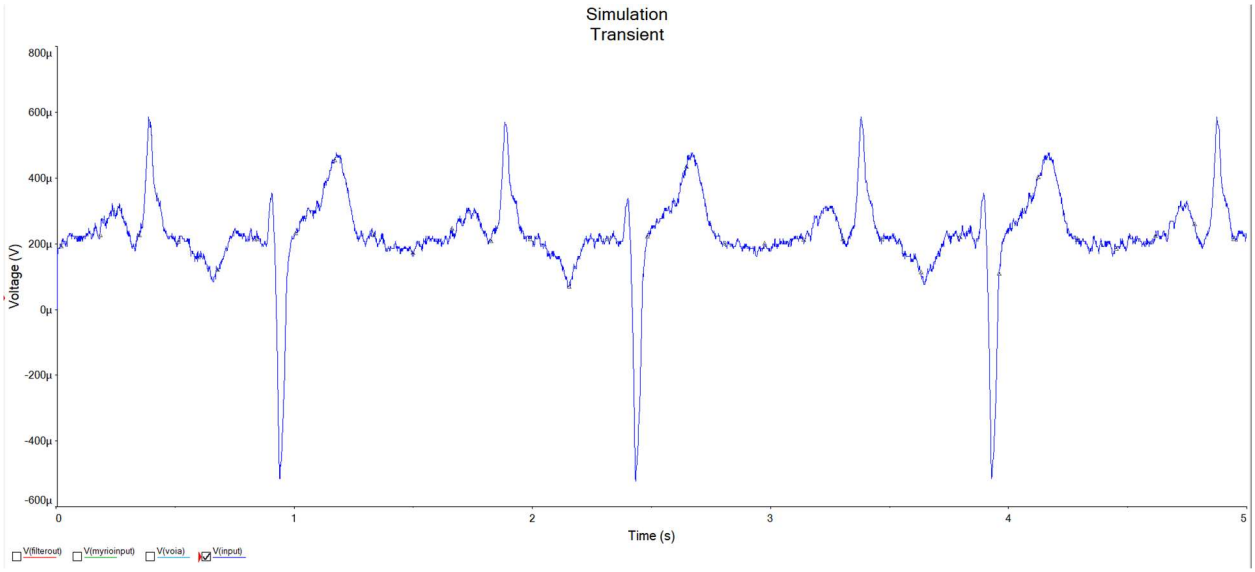

Figure 1.6: EKG Original Signal

The figure below displays various stages of the circuit compared to the input signal. The blue signal is the output of the instrumentation amplifier after the gain has been applied. The red signal represents the signal after it goes through the anti-aliasing filter. The green signal is the output of the isolator which would become the input for the MyRio when the board is actually tested with a person's heartbeat. The y-axis is shown in the volts scale as opposed to the microvolts scale the original signal was in.

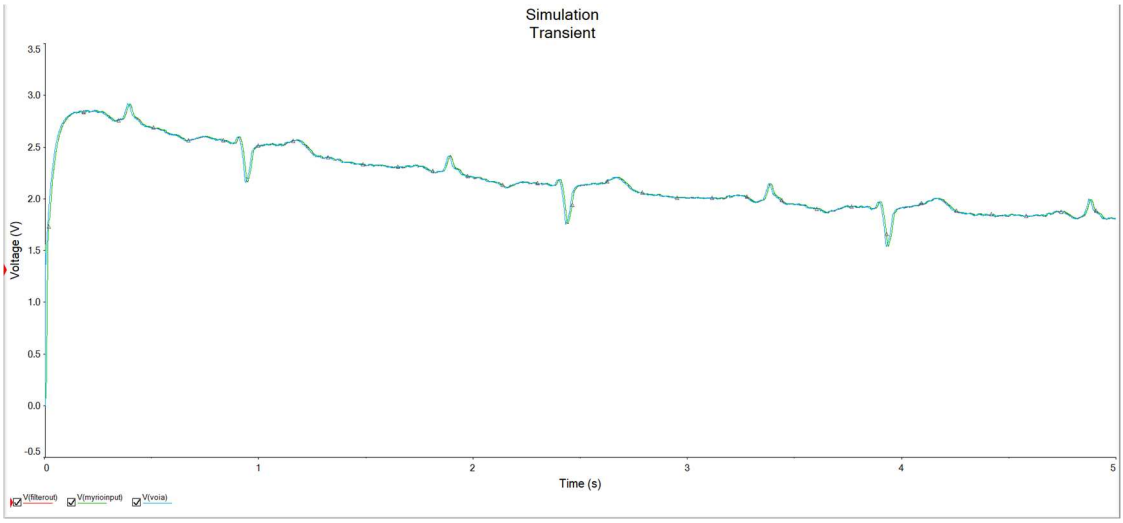

Figure 1.7: Signal at Various Stages

Frequency Domain

The following AC sweeps confirm the cut off frequency to be around 62.9 Hz and a gain of -72 dB around 500 Hz.

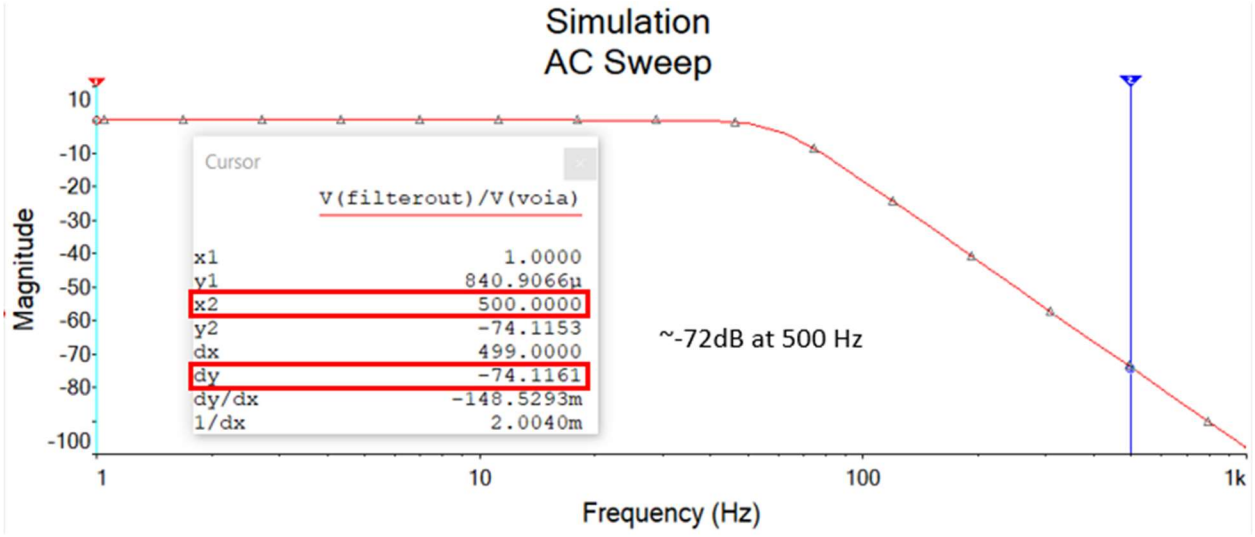

Figure 1.8: AC Sweep Cutoff Frequency

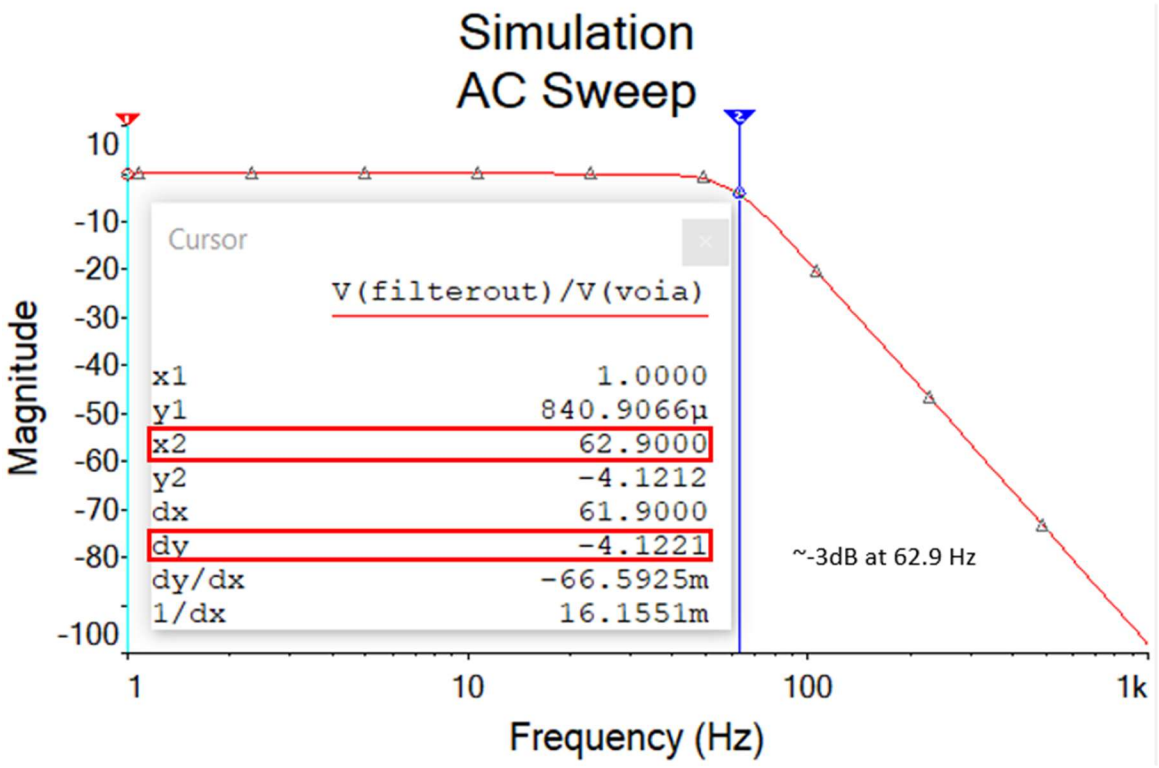

Figure 1.9: AC Sweep 500 Hz

Layout

Silkscreen Top

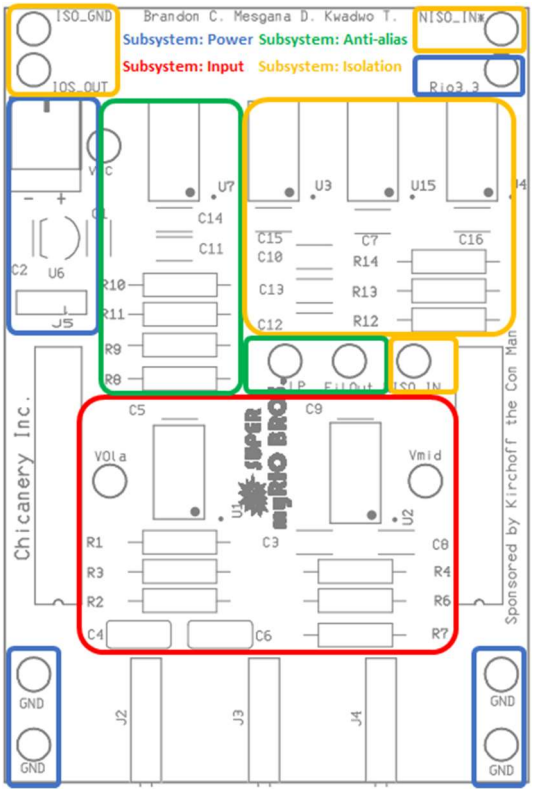

Figure 1.10: Silkscreen Top - Subcomponents

This is the silkscreen top for the project board. It gives a high level look at the component layout for the board, which was very important in ensuring the board performed as intended. The blue section is the power subsystem and was designed with good power practices in mind with thicker traces to reduce inductance along the power lines. The red section is the input section and is composed of the input RC network, instrumentation amplifier and integrator all placed in proximity to each other. The green section is the anti-aliasing subsystem and the yellow section is the isolator subsystem. The test points were placed close to the subsystems that they test and were labeled for easier identification.

Copper Top

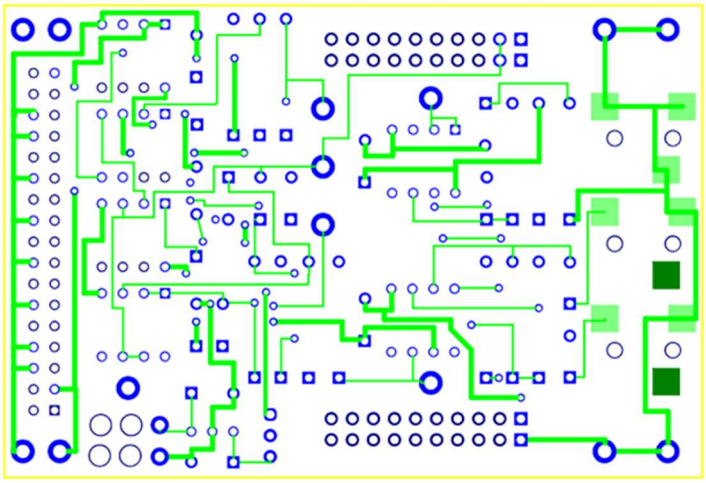

Figure 1.11: Copper Top

The top layer contains predominantly vertical traces in order to keep the board layout clean. Additionally, the power lines were made thicker in order to reduce inductance along them.

Copper Bottom

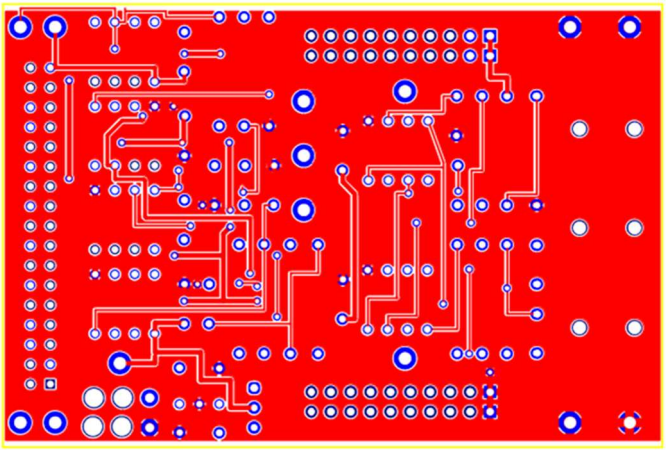

FIgure 1.12: Copper Bottom

A ground power plane was added to the copper bottom to reduce the effect of inductance along traces. Additionally the traces are predominantly vertical in order to keep the board clean.

Board Selection

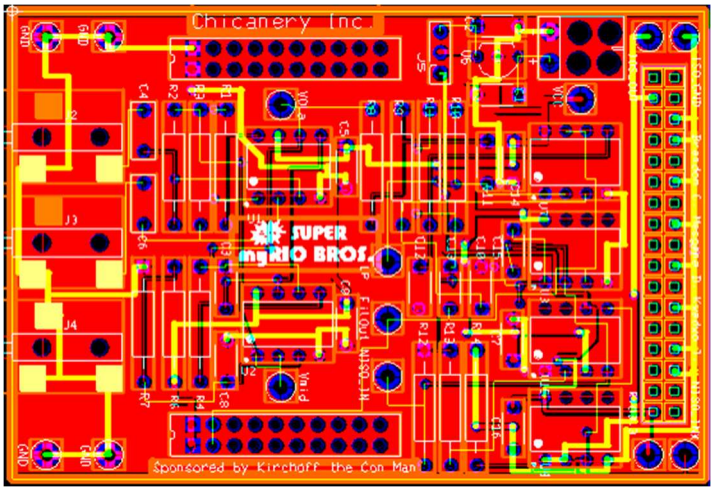

Figure 1.13: Final Board Design

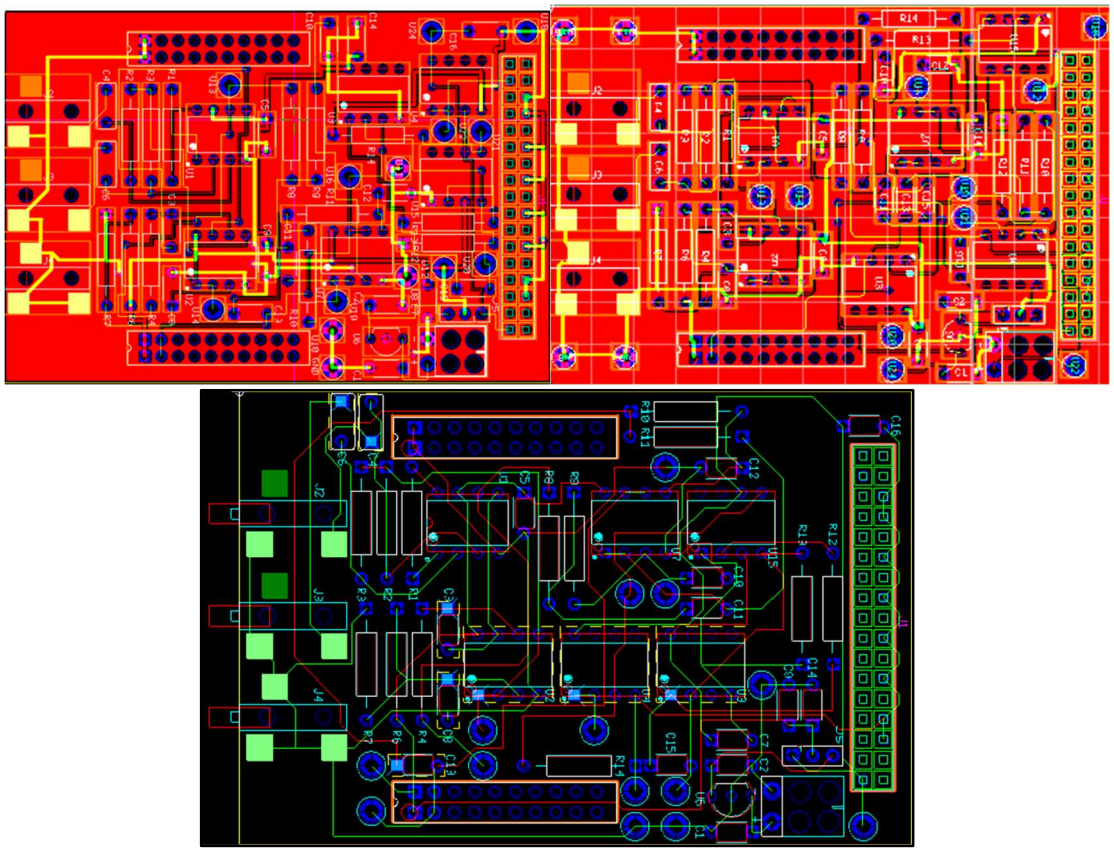

Figure 1.14: Other Board Options

This board was chosen because it stood out for a few reasons. This board was neatly routed and laid out in a way that contributed to good power practices. The power and ground lines were thicker in order to reduce inductance along traces and the power components were placed

relatively close to their traces to reduce the distance. Additionally the team agreed with the test point placing convention on this board where the test points were placed close to the components they tested and labeled to represent the nets they tested. Furthermore, the resistors and capacitors were placed in a logical fashion, around the op amp configurations they were part of.

Manufacturing

In order to ensure the manufactured board would be free of errors, the team implemented some key procedures. First, Ultiboard's built-in Design Rules Checklist (DRC), Connectivity and Netlist Check was run to confirm all connections were made and design standards were met. Finally, the board was submitted to FreeDFM, a website that runs additional checks for board manufacturability. Since the website required Gerber Files, the Ultiboard files were converted using a tool provided. Initially there were issues with insufficient trace and spacing where some traces were made too closely to certain vias. Once these were addressed, the board was cleared for manufacturing.

Figure 1.15: FreeDFM Results

Testing and Implementation

To begin the testing process we first outlined the planned procedure for verifying that each subsystem functions as designed. These procedures and their expected outcomes are annotated below in Table 1.

Test Order	Subsystem	Test	Setup	Expected Output
1	Power Supply	3.3V Out	A digital multimeter will be attached to the power supply output.	The expected output is a DC voltage at around 3.3 Volts with an error of ±0.1 Volts
2	VMID	1.65V Out	Pass 3.3V into R6 via VB power supply and measure output using DMM	1.65 V expected at output of Opamp
3	Isolator	Unity gain	Two oscilloscopes will be hooked up to the input and output of the isolator. An AC sweep will be performed to determine if each op amp functions as intended by design.	A bode plot that resembles a constant that has the magnitude of 0dB
4		Max LED current	An oscilloscope will be used to measure the output of the isolator circuit.	The maximum voltage is outputted at 3.3V.

5	Antialiasing Filter	-72dB at 500Hz	Two oscilloscopes will be hooked up to the input and output of the antialiasing filter. An AC sweep will be performed to see if the measured bode plot matches the expected results.	A low pass filter with approximately -72 dB attenuation at 500 Hz.
6	Integrator	Pole at 0 Hz and constant gain between: $-1 < G < -\frac{1}{10}$	Two oscilloscopes will be placed on the input and output of the integrator. An AC Sweep will be performed.	The attenuation at -20 db/decade begins immediately and the constant it starts at is -20 dB
7	Instrumentation Amplifier	Corner frequency between 0.05Hz and 0.1 Hz	Two oscilloscopes will be placed on the input and output of the instrumentation amplifier. Labview's Bode plot tool will be run to confirm 0.05 Hz and 0.1 Hz corner frequency.	The corner frequency is determined by measurements to be within 0.05 Hz and 0.1 Hz.
8		P-P of 1.5 to 2.5 for EEG	Using LVM to VB, send EEG file through Vsig+ with Vsig- grounded	Output shows an undistorted heartbeat with little interference.

Table 2.0: Testing Plans and Expected Results

Subsystem: Power Supply

To test the power supply we began by recreating the configuration of the voltage regulator on a breadboard. This configuration is shown in Figure 2.1. Thereafter we then plugged in a 9 volt battery into the breadboard circuit configuration.

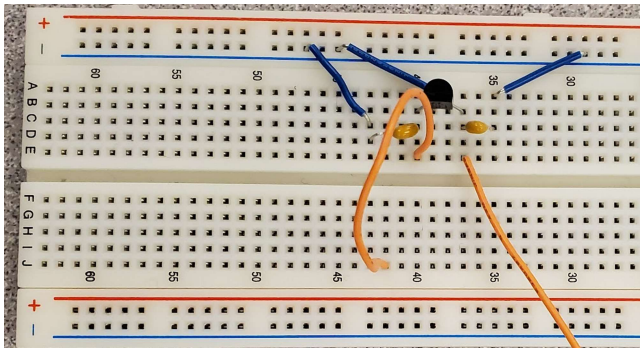

Figure 2.1: Picture of Voltage Regulator Test

The measurement of the input voltage is shown in Figure 2.2.

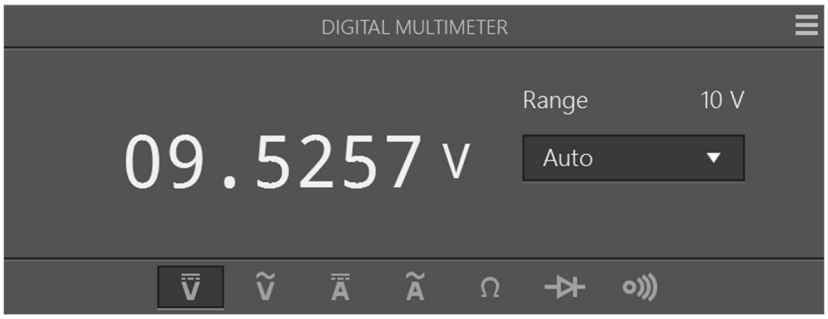

Figure 2.2: Input Voltage 9 Volt Battery

The resulting measured output voltage from the power regulator is shown in Figure 2.3.

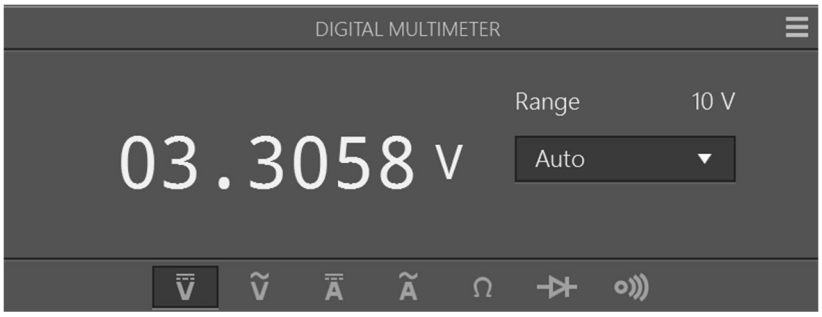

Figure 2.3: Output Voltage From Regulator

As evident from Figure 2.3 the measured voltage is as expected and is within error range of the voltage regulator.

Subsystem: Input

Integrator

For testing the integrator, we first recreated the circuit on a breadboard with our solved components. Thereafter once this circuit was recreated, we attempted to use the LabView Bode Analyzer in order to determine that the measured bode plot of the built circuit resembled the expected theoretical bode plot. However, once we attempted to use the LabView Bode Analyzer we encountered an error in the program which resulted in a visually wrong bode plot.

Thereafter we altered our testing strategy to instead verify that the circuit is functioning as an integrator. To do this we inputted a low frequency square wave at 0.1 Hz with an amplitude of 3.30 Volts and a DC offset of 1.65 Volts. By inputting a low frequency square wave, we can verify that the circuit is successfully integrating the input voltage.

Shown in Figure 2.4 is the input voltage, represented by Channel 1, and the output voltage of the circuit, represented by Channel 2.

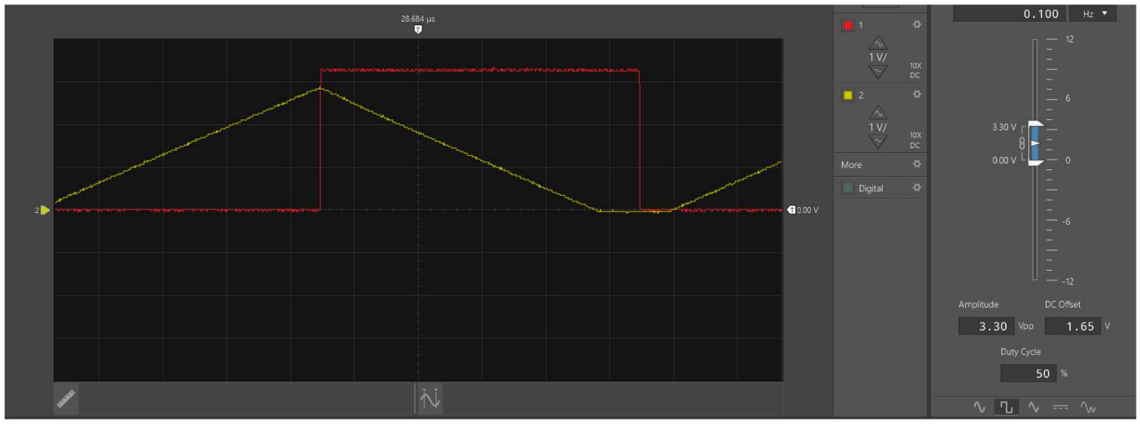

Figure 2.4: Built Integrator Input and Output Voltage

As evident from Figure 2.4 the square wave is successfully being integrated. The output voltage resembles a triangle wave. This therefore confirms that the circuit is functioning as an integrator.

Instrumentation Amplifier

For the instrumentation amplifier, we first began by assembling the circuit on a breadboard. This circuit strictly included the instrumentation amplifier and did not include the integrator in a feedback configuration. However, we did include the RC Network as shown in Figure 2.5.

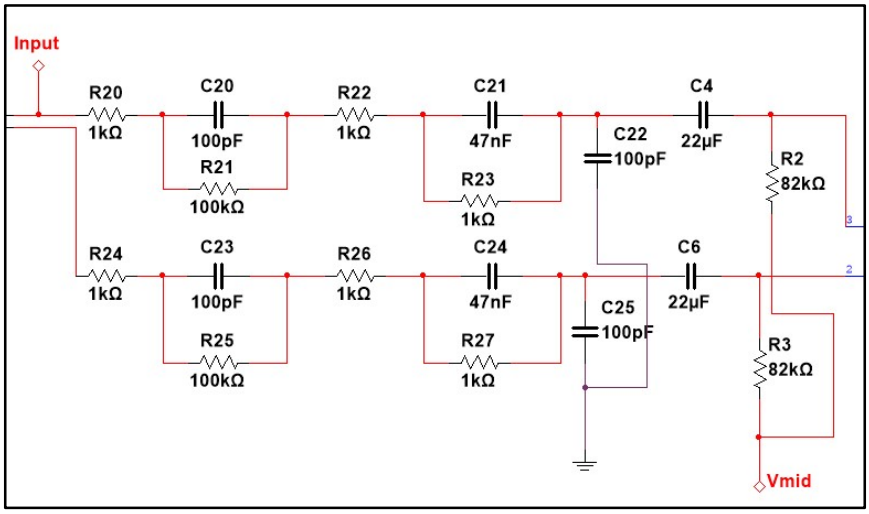

Figure 2.5: RC Network Layout

In order to simulate the circuit's behavior with a heartbeat, we used the provided LVM files as an input to the built circuit. Shown in Figure 2.6 is the output of the instrumentation amplifier compared to the function generator's input voltage.

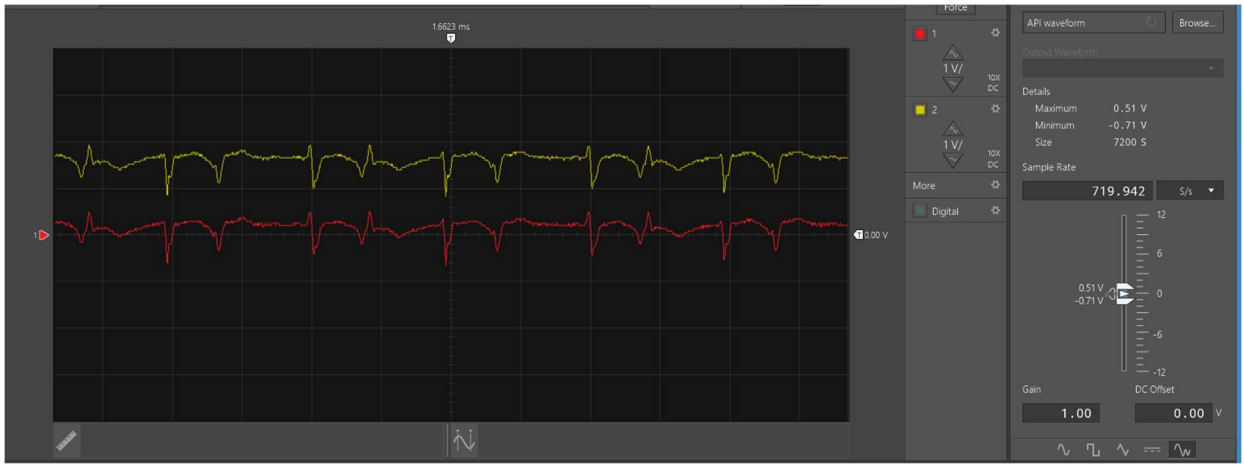

Figure 2.6: Input Voltage Compared to Instrumentation Amplifier Output

Shown in Figure 2.6, the output voltage of the instrumentation amplifier is shown to be successfully free of any unwanted noise and the DC offset is at V_{MID}. This therefore proves our instrumentation amplifier is functioning as intended.

Subsystem: Isolator

To test the isolator we just want to make sure that the input of the isolator and the output of the isolator match. First, we setup the correct circuit on a breadboard to make sure the components work before soldering them onto the PCB. The correctness was verified by inputting the simulated lvm heartbeat measured on channel one and the output of the isolator on channel two with is shown in Figure 2.7.

Figure 2.7: Breadboard Isolator test

Then the components were put onto the PCB board and the setup shown in Figure 2.8 was done to do the same test that was implemented on the breadboard and Figure 2.9 is the results which correctly follow the inputted result.

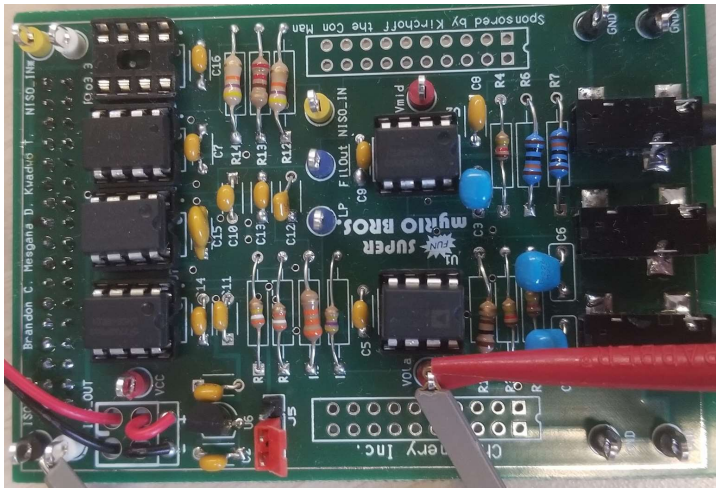

Figure 2.8: PCB test for Isolator Output

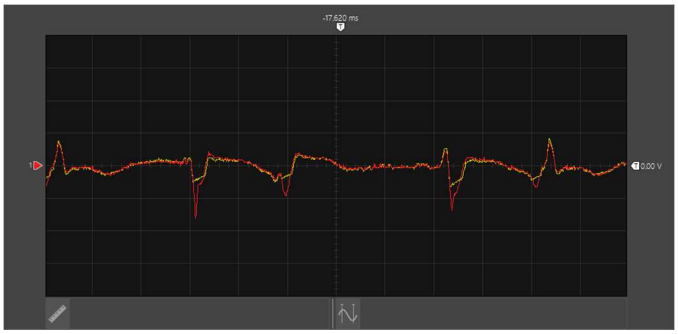

Figure 2.9: PCB Isolator test

Subsystem: Anti-Aliasing Filter

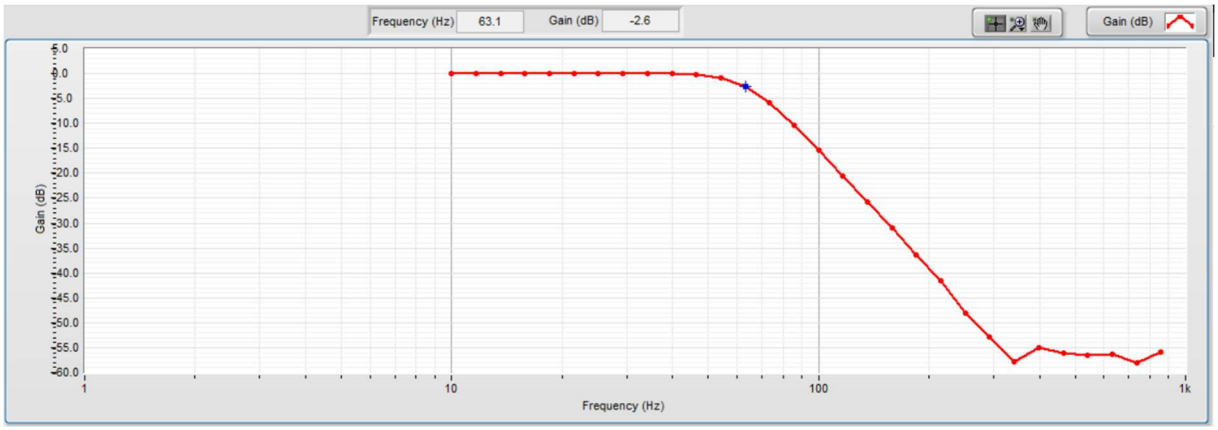

Figure 2.10: Anti-Aliasing Filter Test on Breadboard

After constructing the 4th order butterworth filter on a breadboard as designed in the section above, the following bode plot was created using a bode tool from LabView. From the figure, it can be seen that the correct -3dB frequency occurred at 63Hz and there was unity gain.

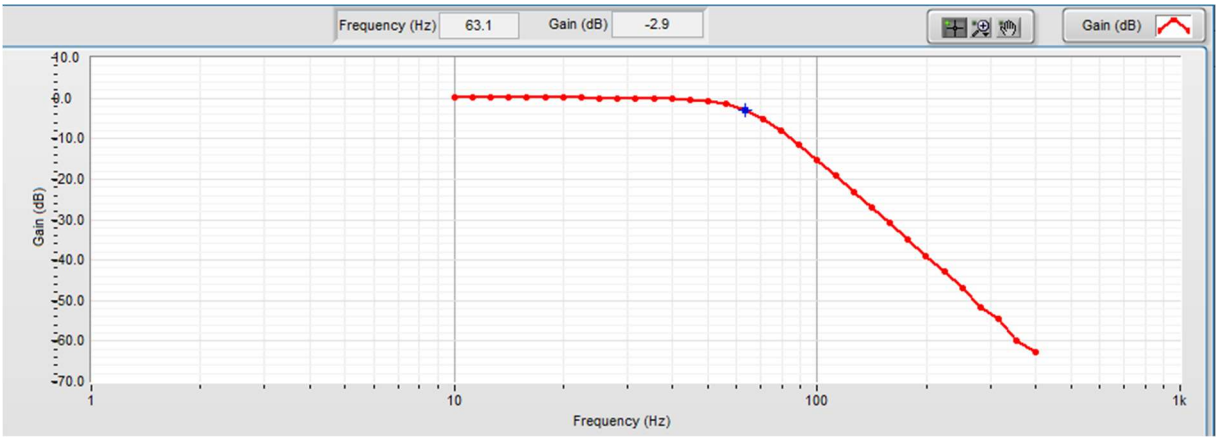

Figure 2.11: Anti-Aliasing Filter Test on PCB

Once the components designed produced the intended behavior for the anti-aliasing filter as shown by the breadboard test in Figure 2.11, the components were soldered onto the PCB board. The bode plot was then reran and the -3dB frequency was at 63Hz as designed, but instead of -72dB attenuation at 500Hz, the attenuation was at about -52dB. This is possibly due to the test being ran on the PCB where other components were connected and not isolated like on the breadboard.

Full System

Using the LVMtoVB application, the EKG signal that was used during the Multisim simulations was sent through the input of the PCB board with the Channel 1 oscilloscope connected. The output of the isolator which is the output of the system (and input for the MyRio), was recorded with the Channel 2 oscilloscope.

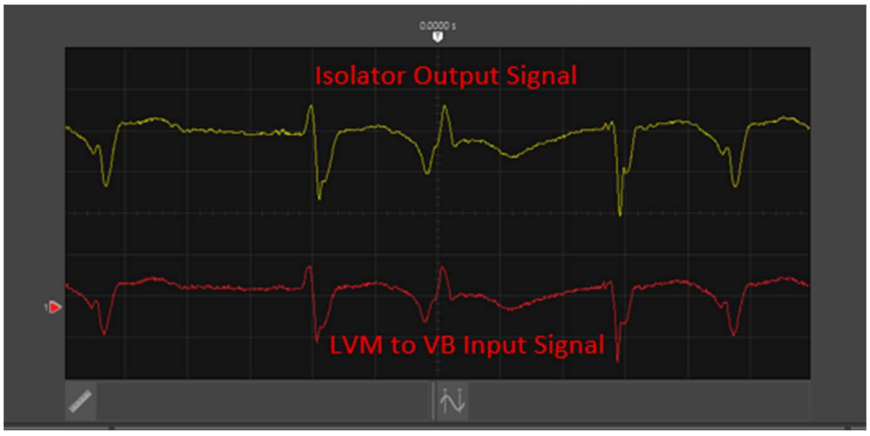

Figure 2.12: Full System LVMtoVB Signal Test

Since testing the full system returns an output signal that matches the input LVMtoVB signal, electrodes were placed on one of the team members which were inputted into the PCB board.

Below, the Channel 2 oscilloscope records the output of the full system which is the heartbeat signal of the team member with visible heartbeats displayed.

Figure 2.13: Full System Heartbeat Signal

Conclusion

Summary

The project was a success. The test driven development used helped the team catch errors early and finish the project on time. By building and testing each subsystem separately, first on a breadboard then soldering onto the PCB, we were able to streamline the construction by running several stages in parallel. Additionally, the ability to run simulations in Multisim greatly helped by allowing for capacitor and resistor values to be tested and modified before running tests with physical components.

To achieve the goal of this project, which was to isolate and amplify the electric signal generated by the heart, we used a variety of analog circuitry and digital signal processing techniques we learned throughout the semester.

In order to isolate and detect the signal coming from the heartbeat we used an instrumentation amplifier to amplify the difference between the two probes and eliminate the common mode voltage in the output signal. This allowed for the heartbeat to be successfully isolated. Due to the voltage range of the analog components in the circuit being between 0 and 3.3 Volts, we also made sure to DC bias the isolated heartbeat by 1.65 Volts.

However, to improve the performance of the instrumentation amplifier and reduce the noise present in the output signal even further we added a high-pass RC filter between the probes and the instrumentation amplifier inputs. This allowed us to attenuate any unwanted low frequency

noise. Furthermore, we attached an integrator in a feedback configuration to the instrumentation amplifier to reduce and prevent errors from propagating in the output signal.

Thereafter with the heartbeat isolated and error reduced, we then passed the signal from the instrumentation amplifier to an anti-aliasing filter. This anti-aliasing filter reduced any unwanted high frequency signals from aliasing and showing up within the frequency range of interest. After this, we then passed the signal to an isolator. This isolator allowed us to provide a physical barrier between the myRIO used for digital signal processing, which operates using 120V AC power and the rest of the circuit. This physical barrier was made possible by an internal LED and photodiode within the isolator chip. This setup allows for the information to be communicated without any physical connections. By having this physical barrier, we reduced the risk of any unwanted short circuits in the myRIO from creating a lethal shock that could travel through the voltage probes and into the body of the user.

The isolator then passed the signal of the heartbeat to a myRIO module. Thereafter we then used a digital moving averaging filter to eliminate the 60 Hz noise that is prevalent in real life. Once the 60 Hz noise was eliminated, the signal was ready to be recorded and displayed.

Improvement

One of the improvements that can be made for this project is to increase the size of the PCB board. When placing components and making traces on the board in the Ultiboard application, the size of the board caused putting the components in suboptimal locations as there was barely enough space for all the components which resulted in lengthy, inefficient traces. Furthermore, an additional improvement is to allot more time for this project to be worked on in class as the combination of also having to do the three LabVIEW wikis lead to multiple groups scrambling to finish the project near the report due date.

Appendix

Digital Signal Processing (DSP)

A myRIO was used to digitally process the signal coming from the EKG using code given in LabView. From the original time domain signal, it can be seen that there is a consistent 60Hz noise signal present. Using a moving average filter, also given to us, the 60Hz is nearly eliminated. This elimination can be seen more clearly on the FFT produced spectrum, where strong attenuation is present in the spectrum at multiples of 60Hz.

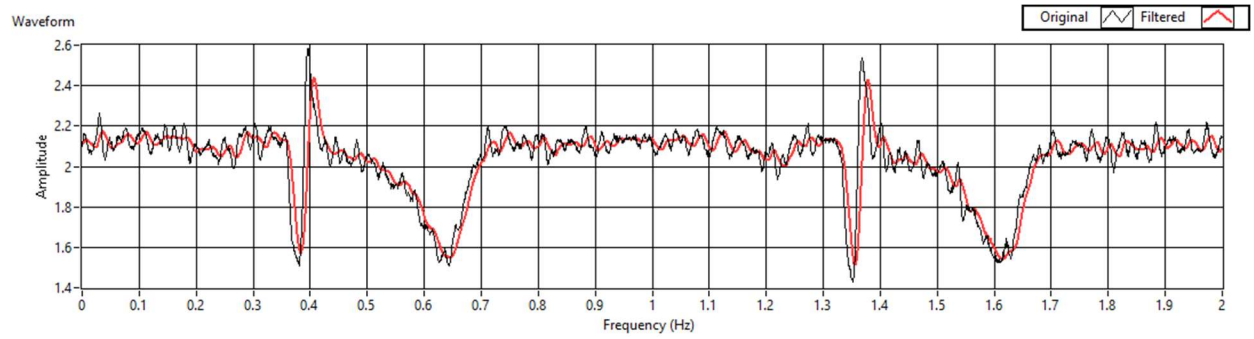

Figure 3.0: Time Domain Original and Filtered

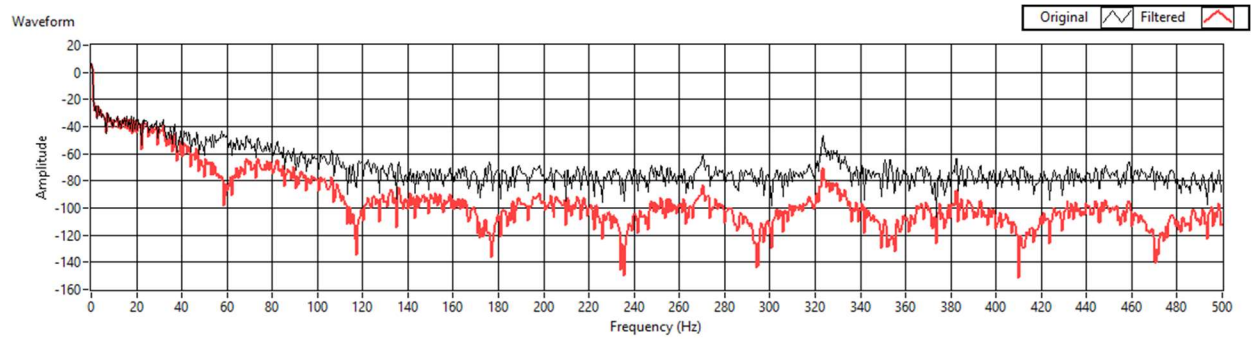

Figure 3.1: Spectrum Original and Filtered

Extra Credit: Implementing an FIR Filter

To develop a filter to eliminate the 60Hz interference, a kernel of 17 1/17 was implemented. Since the sampling frequency was 1kHz and we need to eliminate the 60 Hz frequency, 60/1000≈ 1/17. This was then convolved with the unfiltered csv signal. The results shown in Figure 3.2 and Figure 3.3 display both the unfiltered and filtered signal to mimic Figure 3.0.

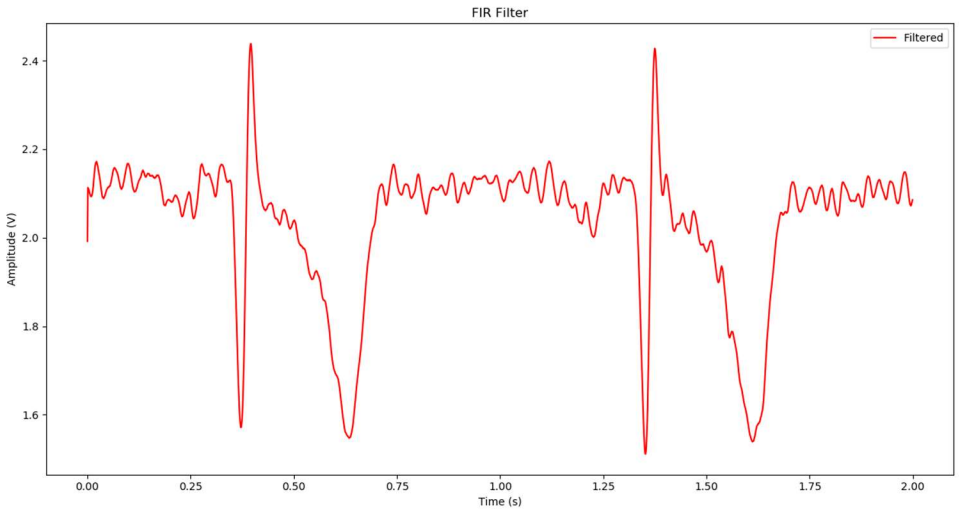

Figure 3.2: FIR Filtered Signal

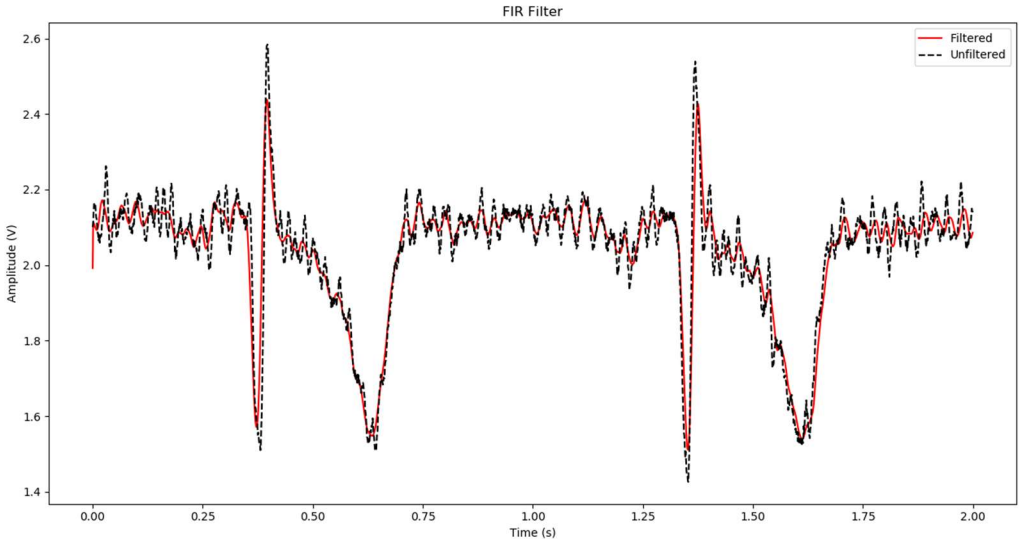

Figure 3.3: FIR vs Original Signals

Printed Circuit Board (PCB)

Figure 3.4: Final Board (bottom)
Figure 3.5: Final Board (top)